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06ES32

Third Semester B.E. Degree Examination, June / July 08
Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions, selecting atleast two questions from each part.***

PART A

1 a. Differentiate between static and dynamic resistance of a semi conductor diode. **(04 Marks)**

b. Explain with the help of a circuit diagram the working of a Full Wave Rectifier. Derive expressions for i) I_{dc} ii) I_{rms} iii) V_{dc} iv) Ripple factor v) Rectifier efficiency. **(10 Marks)**

c. For the circuit shown, in Fig.Q1(c) write the transfer characteristic equations. Assume diodes are ideal. Plot V_0 against V_i, indicating all slopes and voltage levels. **(06 Marks)**

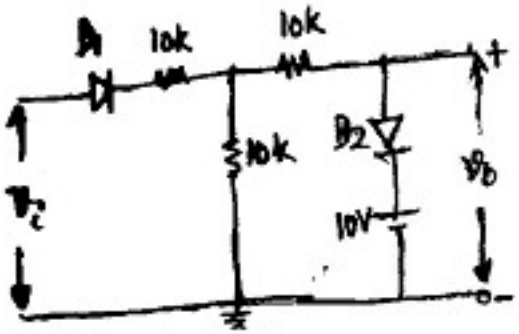

Fig.Q1(c)

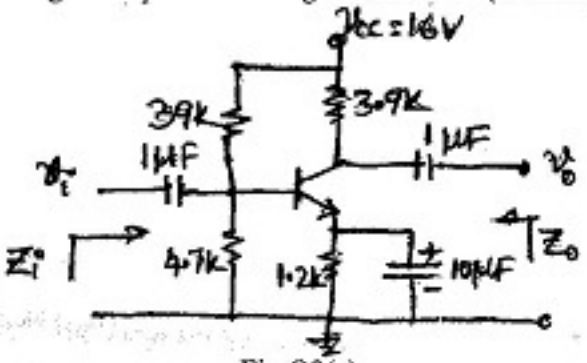

Fig.Q3(a)

2 a. Design a voltage divider bias circuit with V_{CC} = 10 V, R_C = 1.5 K ohm, I_C = 2 mA, V_{CE} = 5 V, β = 50. Assume silicon transistor and stability factor S = 5. **(08 Marks)**

b. Derive an expression for the stability factor $S(I_{CO})$ for a voltage divider bias circuit. **(08 Marks)**

c. Determine R_B and R_C for the transistor inverter of Fig.Q2(c) if I_{Csat} = 10 mA. **(04 Marks)**

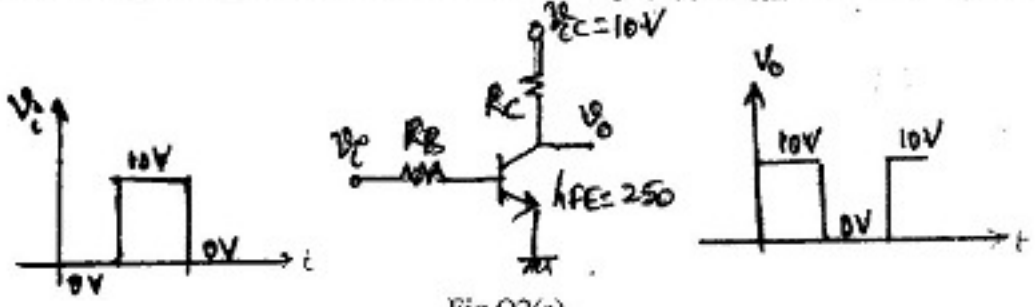

Fig.Q2(c)

3 a. For the network of Fig.Q3(a): i) Determine r_e ii) Calculate Z_i and Z_0 iii) Find A_V Given β = 100 S_i transistor. **(08 Marks)**

b. Draw the emitter follower circuit. Derive expressions for:
i) Z_i ii) Z_0 iii) A_V using r_e model. **(08 Marks)**

c. Define h-parameters. Draw the h-parameter model of a transistor. **(04 Marks)**

4 a. Determine the lower cutoff frequency for the network of Fig.Q4(a). Given β = 100, r_s = ∞ ohm. Determine the mid band gain. If C_{be} = 36 pF, C_{bc} = 4 pF, C_{w_i} = 6 pF, C_{w_o} = 8 pF. Determine f_{H_i} and f_{H_o} and sketch the frequency response for low and high frequency regions using the results. **(12 Marks)**

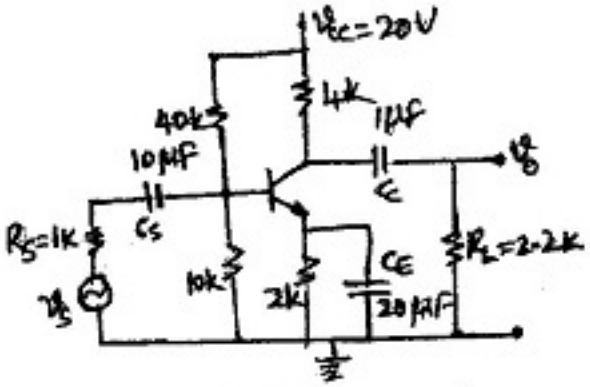

Fig.Q4(a)

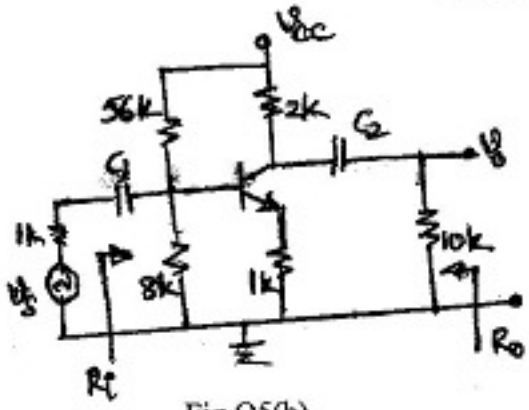

Fig.Q5(b)

b. Calculate the overall lower 3 db and upper 3 db frequencies for a 3 stage amplifier having an individual $f_1 = 40$ Hz and $f_2 = 2$ MHz. **(08 Marks)**

PART B

5 a. Draw the cascade configuration and list the advantages of this circuit. **(04 Marks)**

b. Determine A_i, R_i, A_v and R_0 for the circuit shown in fig.Q5(b). Given h parameters $h_{ie} = 1.1$ k ohm, $h_{re} = 2 \times 10^{-4}$, $h_{oe} = 25 \times 10^{-6}$ ℧, $h_{fe} = 50$. **(08 Marks)**

c. List the advantages of negative feedback amplifier. Derive expressions for Z_{if} and Z_{of} for voltage series feedback amplifier. **(08 Marks)**

6 a. Explain the working of a class B push pull amplifier. Prove that the maximum efficiency is 78.5%. **(10 Marks)**

b. A single transistor amplifier with transformer coupled load produces harmonic amplitudes in the output as $B_0 = 1.5$ mA, $B_1 = 120$ mA, $B_2 = 10$ mA, $B_3 = 4$ mA, $B_4 = 2$ mA, $B_5 = 1$ mA. i) Determine the percentage total harmonic distortion

ii) Assume second identical transistor is used along with suitable transformer to provide push pull operation. Using the above harmonic amplitudes, determine the new total harmonic distortion. **(10 Marks)**

7 a. Explain with the help of a circuit diagram, the working of an RC phase shift oscillator. **(08 Marks)**

b. With the help of Barkhousen criterion, explain the working of a BJT crystal oscillator. **(08 Marks)**

Calculate the frequency of a Wien Bridge oscillator circuit when R = 12 k ohm and C = 2400 pf. **(04 Marks)**

8 a. Determine Z_i, Z_0 and A_v for the circuit shown in Fig.Q8(a), if Y_{fs} = 3000 μs and $Y_{os} = 50$ μs. **(06 Marks)**

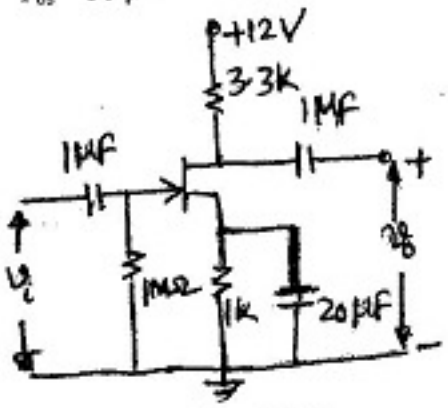

Fig.Q8(a)

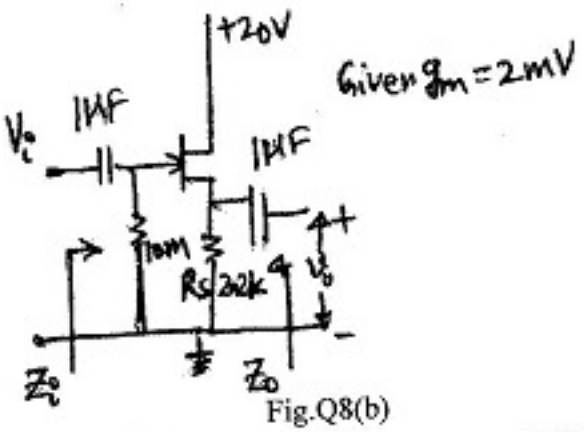

Fig.Q8(b)

b. Determine Z_i, Z_0, and A_v if $r_d = 40$ kΩ for fig.Q8(b). **(06 Marks)**

c. With the help of circuits and equations, show different biasing arrangements for depletion type MOSFET. **(08 Marks)**

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